Exhibit 1

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Mo et al.

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(54) **FIELD EFFECT TRANSISTOR AND METHOD OF ITS MANUFACTURE**

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(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(22) Filed: **Nov. 14, 1997**

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(52) **U.S. Cl.** **257/341**; 257/331
(58) **Field of Search** 257/330, 245, 257/497, 618, 341, 331

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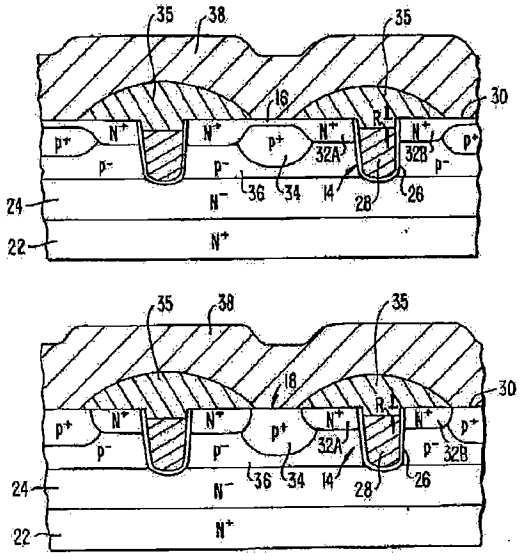
(57) **ABSTRACT**

A trenched field effect transistor is provided that includes (a) a semiconductor substrate, (b) a trench extending a predetermined depth into the semiconductor substrate, (c) a pair of doped source junctions, positioned on opposite sides of the trench, (d) a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of the heavy body extending less deeply into said semiconductor substrate than the predetermined depth of the trench, and (e) a doped well surrounding the heavy body beneath the heavy body.

22 Claims, 9 Drawing Sheets



The next two steps (p+ heavy body formation) can be performed either before formation of the n+ source junction, or afterwards, as indicated by the arrows in FIG. **3**. P+ heavy body formation and n+ source junction formation can be performed in either order because they are both resist-masked steps and because there is no diffusion step in between. This advantageously allows significant process flexibility. The p+ heavy body formation steps will be described below as being performed prior to source formation; it will be understood that n+ source formation could be performed first simply by changing the order of the steps discussed below.

First, a mask is formed over the areas that will not be doped to p+, as shown in FIG. **4***h*. (It is noted that this masking step is not required if the p+ heavy body is formed later, after the dielectric layer has been applied and patterned for contact holes. (see FIG. **4***k*, below) so that the dielectric itself provides a mask.) As discussed above, it is preferred that the junction at the interface between the p− well and the p+ heavy body be abrupt. To accomplish this, a double implant of dopant (e.g., boron) is performed. For example, a preferred double implant is a first boron implant at an energy of 150 to 200 keV and a dose of 1E15 to 5E15, and a second boron implant at an energy of 20 to 40 keV and a dose of 1E14 to 1E15. The high energy first implant brings the p+ heavy body as deep as possible into the substrate, so that it will not compensate the n+ source junction to be introduced later. The second, lower energy/lower dose implant extends the p+ heavy body from the deep region formed during the first implant up to the substrate surface to provide the p+ contact **18**. The resulting p+ heavy body junction is preferably about 0.4 to 1 μm deep at this stage of the process (final junction depth after drive-in is preferably about 0.5 to 1.5 μm deep), and includes a region of high dopant concentration near the interface with the p− well, and a region of relatively low dopant concentration at the contact surface of the p+ heavy body. A preferred concentration distribution is shown in FIG. **5**.

It will be appreciated by those skilled in the art that the abrupt junction can be formed in many other ways, e.g., by diffused dopants, by using a continuous dopant source at the surface or by using atoms that diffuse slowly.

After the formation of the p+ heavy body, a conventional resist strip process is performed to remove the mask, and a new mask is patterned to prepare the substrate for the formation of the n+ source junction. This mask is a n+ blocking mask and is patterned to cover the areas of the substrate surface which are to provide p+ contacts **18** (FIGS. **1** and **1***b*), as shown in FIG. **4***i*. This results in the formation of alternating p+ and n+ contacts after n-type doping (see lines A—A and B—B and cross-sectional views A—A and B—B in FIG. **4***i*, which correspond to FIGS. **1***a* and **1***b*).

The n+ source regions and n+ contact are then formed using a double implant. For example, a preferred double implant process is a first implant of arsenic at an energy of 80 to 120 keV and a dose of 5E15 to 1E16 followed by a second implant of phosphorus at an energy of 40 to 70 keV and a dose of 1E15 to 5E15. The phosphorus implant forms a relatively deep n+ source junction, which allows more process flexibility in the depth of the polysilicon recess, as discussed above. Phosphorus ions will penetrate deeper into the substrate during implant and also during later diffusion steps. Advantageously, the n+ source regions will have a depth of about 0.4 to 0.8 μm after diffusion. The arsenic implant extends the n+ source to the substrate surface, and also forms the n+ contacts **16** (see FIGS. **1** and **1***a*) by compensating (converting) the p-type surface of the p+ heavy body to n-type in the desired contact area. The preferred sheet resistance profiles for the n+ source along the edge of the trench, and the n+ contact are shown in FIGS. **5***a* and **5***b*, respectively.

Thus, the alternating p+ and n+ contacts **18**, **16**, shown in FIG. **1** are formed by patterning the substrate with appropriate masks and doping with the first p+ implant and the second n+ implant, respectively, as described above. This manner of forming the alternating contacts advantageously allows an open cell array having a smaller cell pitch than is typical for such arrays and thus a higher cell density and lower Rds_{on}.

Next, a conventional n+ drive is performed to activate the dopants. A short cycle is used, preferably 10 min at 900° C., so that activation occurs without excessive diffusion.

A dielectric material, e.g., borophosphate silicate glass (BPSG), is then deposited over the entire substrate surface and flowed in a conventional manner (FIG. **4***j*), after which the dielectric is patterned and etched (FIG. **4***k*) to define electrical contact openings over the n+ and p+ contacts **16**, **18**.

As noted above, the p+ heavy body implant steps can be performed at this point, if desired (rather than prior to n+ source formation), eliminating the need for a mask and thus reducing cost and process time.

Next, the dielectric is reflowed in an inert gas, e.g., a nitrogen purge. If the p+ body has been implanted immediately prior, this step is required to activate the p+ dopant. If the p+ body was implanted earlier, prior to the n+ drive, this step can be omitted if the dielectric surface is sufficiently smooth-edged around the contact openings.

The cell array is then completed by conventional metalization, passivation deposition and alloy steps, as is well know in the semiconductor field.

Other embodiments are within the claims. For example, while the description above is of an n-channel transistor, the processes of the invention could also be used to form a p-channel transistor. To accomplish this, "p" and "n" would simply be reversed in the above description, i.e., where "p" doping is specified above the region would be "n" doped instead, and vice versa.

What is claimed is:

1. A trenched field effect transistor comprising:

a semiconductor substrate having dopants of a first conductivity type;

a trench extending a predetermined depth into said semiconductor substrate;

a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;

a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a depth that is less than said predetermined depth of the trench; and

a doped heavy body having dopants of the second conductivity type, and positioned adjacent each source junction on the opposite side of the source junction from the trench, said heavy body extending into said doped well to a depth that is less than said depth of said doped well,

wherein the heavy body forms an abrupt junction with the well and the depth of the junction, relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.

2. The trenched field effect transistor of claim 1 wherein said doped well has a substantially flat bottom.

3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.

4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.

5. The trenched field effect transistor of claim 4 wherein said doped heavy body has a first dopant concentration near the abrupt junction and a second dopant concentration near its upper surface that is less than the first dopant concentration.

6. An array of transistor cells comprising:

a semiconductor substrate having a first conductivity type;

a plurality of gate-forming trenches arranged substantially parallel to each other, each trench extending a predetermined depth into said substrate and the space between adjacent trenches defining a contact area;

a pair of doped source junctions, positioned on opposite sides of the trench and extending along the length of the trench, the source junctions having the first conductivity type;

a doped well having a second conductivity type with a charge opposite that of the first conductivity type, the doped well formed in the semiconductor substrate between each pair of gate-forming trenches;

a doped heavy body having the second conductivity type formed inside the doped well and positioned adjacent each source junction, the deepest portion of said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trenches; and

alternating heavy body and source contact regions defined at the surface of the semiconductor substrate along the length of the contact area,

wherein the heavy body forms an abrupt junction with the well, and a depth of the heavy body relative to a depth of the well is adjusted so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor.

7. The array of transistor cells of claim 6, wherein each said doped well has a substantially flat bottom.

8. The array of transistor cells of claim 6 wherein the controlled depth of the junction causes the breakdown origination point to occur approximately halfway between adjacent gate-forming trenches.

9. The array of transistor cells of claim 6 wherein each said doped well has a depth less than the predetermined depth of said gate-forming trenches.

10. The array of transistor cells of claim 6 wherein each said gate-forming trench has rounded top and bottom corners.

11. The array of transistor cells of claim 9 further comprising a field termination structure surrounding the periphery of the array.

12. The array of transistor cells of claim 11 wherein said field termination structure comprises a well having a depth greater than that of the gate-forming trenches.

13. The array of transistor cells of claim 11 wherein said field termination structure comprises a termination trench extending continuously around the periphery of the array.

14. The array of transistor cells of claim 13 wherein said field termination structure comprises a plurality of concentrically arranged termination trenches.

15. A trenched field effect transistor formed on a substrate, comprising:

a plurality of trenches formed in parallel along a longitudinal axis, the plurality of trenches extending into the substrate to a first depth;

a doped well extending into the substrate between each pair of trenches;

a pair of doped source regions formed on opposite sides of each trench; and

a doped heavy body formed inside the doped well adjacent each source region, the doped heavy body extending into the doped well to a second depth that is less than the first depth,

wherein the doped heavy body:

forms a continuous doped region along substantially the entire longitudinal axis of a trench, and

forms an abrupt junction with the well, and a depth of the heavy body junction relative to a maximum depth of the well, is adjusted so that a peak electric field in the substrate is spaced away from the trench when voltage is applied to the transistor.

16. The trenched field effect transistor of claim 15 further comprising source and heavy body contact areas defined on a surface of the substrate between each pair of trenches.

17. The trenched field effect transistor of claim 16 wherein the contact areas alternate between source and heavy body contacts.

18. The trenched field effect transistor of claim 1 further comprising an epitaxial layer having dopants of the first conductivity type, and formed between the substrate and the doped well, with no buried layer formed at an interface between the epitaxial layer and the substrate.

19. The semiconductor die of claim 18 wherein said field termination structure comprises a deep doped well.

20. The trenched field effect transistor of claim 19 wherein said double implant comprises a first high energy implant to reach said second depth, and a second lower energy implant to extend the heavy body from said second depth to substantially a surface of the substrate.

21. The trenched field effect transistor of claim 6, further comprising:

an epitaxial layer having the first conductivity type formed between the substrate and the well, with no buried layer formed at an interface between the epitaxial layer and the substrate.

22. The trenched field effect transistor of claim 15, further comprising:

an epitaxial layer having the first conductivity type formed between the substrate and the well,

wherein the second depth relative to a depth of the well is adjusted to eliminate the need for any layers disposed between the epitaxial layer and the substrate.

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(12) **United States Patent**
Mo

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(54) **METHOD OF MANUFACTURING A FIELD EFFECT TRANSISTOR**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/854,102**

(22) Filed: **May 9, 2001**

(65) **Prior Publication Data**

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Related U.S. Application Data

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(52) **U.S. Cl.** **438/270**; 438/268; 438/269
(58) **Field of Search** 438/270, 272, 438/589, 268, 269

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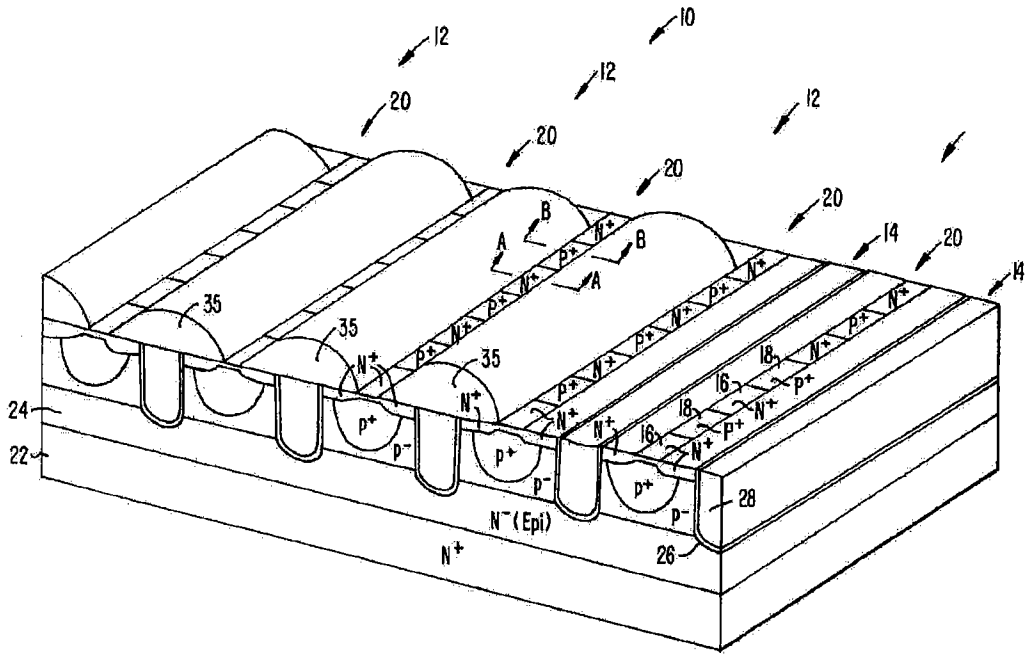
(57) **ABSTRACT**

A method of manufacturing a trenched field effect transistor that includes a heavy body structure. The method includes forming a plurality of trenches into a semiconductor substrate having dopants of a first conductivity type, wherein the gate electrode of the transistor is formed. A doped well having dopants of a second conductivity type is formed into the substrate and between the trenches. Source regions having dopants of the first conductivity type are formed inside the doped well adjacent to and on opposite sides of the trenches. A heavy body region having dopants of the second conductivity type is formed inside each doped well and at a depth that is shallower than the doped well. The heavy body is formed in a manner that makes an abrupt junction between the heavy body and the well. In one embodiment, the abrupt junction is formed by a dobule implant process.

18 Claims, 9 Drawing Sheets



The next two steps (p+ heavy body formation) can be performed either before formation of the n+ source junction, or afterwards, as indicated by the arrows in FIG. **3**. P+ heavy body formation and n+ source junction formation can be performed in either order because they are both resist-masked steps and because there is no diffusion step in between. This advantageously allows significant process flexibility. The p+ heavy body formation steps will be described below as being performed prior to source formation; it will be understood that n+ source formation could be performed first simply by changing the order of the steps discussed below.

First, a mask is formed over the areas that will not be doped to p+, as shown in FIG. 4*h*. (It is noted that this masking step is not required if the p+ heavy body is formed later, after the dielectric layer has been applied and patterned for contact holes. (see FIG. 4*k*, below) so that the dielectric itself provides a mask.) As discussed above, it is preferred that the junction at the interface between the p− well and the p+ heavy body be abrupt. To accomplish this, a double implant of dopant (e.g., boron) is performed. For example, a preferred double implant is a first boron implant at an energy of 150 to 200 keV and a dose of 1E15 to 5E15 cm_2, and a second boron implant at an energy of 20 to 40 keV and a dose of 1E14 to 1E15 cm^{-2}. The high energy first implant brings the p+ heavy body as deep as possible into the substrate, so that it will not compensate the n+ source junction to be introduced later. The second, lower energy/lower dose implant extends the p+ heavy body from the deep region formed during the first implant up to the substrate surface to provide the p+ contact **18**. The resulting p+ heavy body junction is preferably about 0.4 to 1 μm deep at this stage of the process (final junction depth after drive-in is preferably about 0.5 to 1.5 μm deep), and includes a region of high dopant concentration near the interface with the p− well, and a region of relatively low dopant concentration at the contact surface of the p+ heavy body. A preferred concentration distribution is shown in FIG. **5**.

It will be appreciated by those skilled in the art that the abrupt junction can be formed in many other ways, e.g., by diffused dopants, by using a continuous dopant source at the surface or by using atoms that diffuse slowly.

After the formation of the p+ heavy body, a conventional resist strip process is performed to remove the mask, and a new mask is patterned to prepare the substrate for the formation of the n+ source junction. This mask is a n+ blocking mask and is patterned to cover the areas of the substrate surface which are to provide p+ contacts **18** (FIGS. **1** and 1*b*), as shown in FIG. 4*i*. This results in the formation of alternating p+ and n+ contacts after n-type doping (see lines A—A and B—B and cross-sectional views A—A and B—B in FIG. 4*l*, which correspond to FIGS. 1*a* and 1*b*).

The n+ source regions and n+ contact are then formed using a double implant. For example, a preferred double implant process is a first implant of arsenic at an energy of 80 to 120 keV and a dose of 5E15 to 1E16 cm^{-2} followed by a second implant of phosphorus at an energy of 40 to 70 keV and a dose of 1E15 to 5E15 cm^{-2}. The phosphorus implant forms a relatively deep n+ source junction, which allows more process flexibility in the depth of the polysilicon recess, as discussed above. Phosphorus ions will penetrate deeper into the substrate during implant and also during later diffusion steps. Advantageously, the n+ source regions will have a depth of about 0.4 to 0.8 μm after diffusion. The arsenic implant extends the n+ source to the substrate surface, and also forms the n+ contacts 16 (see FIGS. **1** and 1*a*) by compensating (converting) the p-type surface of the p+ heavy body to n-type in the desired contact area. The preferred sheet resistance profiles for the n+ source along the edge of the trench, and the n+ contact are shown in FIGS. 5*a* and 5*b*, respectively.

Thus, the alternating p+ and n+ contacts **18**, **16**, shown in FIG. **1** are formed by patterning the substrate with appropriate masks and doping with the first p+ implant and the second n+ implant, respectively, as described above. This manner of forming the alternating contacts advantageously allows an open cell array having a smaller cell pitch than is typical for such arrays and thus a higher cell density and lower Rds_{on}.

Next, a conventional n+ drive is performed to activate the dopants. A short cycle is used, preferably 10 min at 900° C., so that activation occurs without excessive diffusion.

A dielectric material, e.g., borophosphate silicate glass (BPSG), is then deposited over the entire substrate surface and flowed in a conventional manner (FIG. 4*j*), after which the dielectric is patterned and etched (FIG. 4*k*) to define electrical contact openings over the n+ and p+ contacts **16**, **18**.

As noted above, the p+ heavy body implant steps can be performed at this point, if desired (rather than prior to n+ source formation), eliminating the need for a mask and thus reducing cost and process time.

Next, the dielectric is reflowed in an inert gas, e.g., a nitrogen purge. If the p+ body has been implanted immediately prior, this step is required to activate the p+ dopant. If the p+ body was implanted earlier, prior to the n+ drive, this step can be omitted if the dielectric surface is sufficiently smooth-edged around the contact openings.

The cell array is then completed by conventional metalization, passivation deposition and alloy steps, as is well known in the semiconductor field.

Other embodiments are within the claims. For example, while the description above is of an n-channel transistor, the processes of the invention could also be used to form a p-channel transistor. To accomplish this, "p" and "n" would simply be reversed in the above description, i.e., where "p" doping is specified above the region would be "if" doped instead, and vice versa.

What is claimed is:

1. A method of making a heavy body structure for a trenched DMOS transistor comprising:

providing a semiconductor substrate;

forming a plurality of trenches into the substrate;

implanting a first dopant at a first energy and dosage into the substrate, to form a doped well;

implanting, into said well and between adjacent trenches, a second dopant at a second energy and dosage to form a first doped portion of a heavy body; and

implanting, into said well and between adjacent trenches, a third dopant at a third energy and dosage to form a second doped portion of said heavy body,

wherein the first portion of the heavy body is deeper than the second portion of the heavy body, and wherein said dosage of said second dopant has a doping concentration that is greater than said dosage of said third dopant.

2. The method of claim **1** wherein said first and second dopants both comprise boron.

3. The method of claim **1** wherein said first energy is from about 30 to 100 keV.

4. The method of claim **3** wherein said first dosage is from about 1E13 to 1E15 cm^{-2}.

5. The method of claim **1** wherein said second energy is from about 150 to 200 keV.

6. The method of claim 5 wherein said second dosage is from about 1E15 to 5E15 cm^{-2}.

7. A method of manufacturing a trenched field effect transistor comprising:

forming an epitaxial layer on a semiconductor substrate;

patterning and etching a plurality of trenches into the epitaxial layer;

lining each trench with a gate dielectric layer;

depositing polysilicon to fill the dielectric-lined trenches;

doping the polysilicon with a dopant of a first type;

patterning the epitaxial layer and implanting a dopant of a second, opposite type, in regions between adjacent trenches, to form a plurality of wells interposed between said adjacent trenches;

patterning the epitaxial layer and implanting a dopant of the second type, in regions between adjacent trenches, to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned within the wells;

patterning the epitaxial layer and implanting a dopant of the first type to provide source regions and first dopant type contact areas; and

applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas,

wherein the implanting step for forming the heavy bodies comprises implanting a first dopant at a first energy and dosage and a second dopant at a second energy and dosage, said second energy and dosage being less than said first energy and dosage, respectively.

8. The method of manufacturing a trenched field effect transistor of claim 7 wherein the trenches are patterned to extend in one direction and be substantially parallel to each other.

9. The method of manufacturing a trenched field effect transistor of claim 7 wherein the patterning and implanting steps further comprise arranging the first dopant type contact areas and second dopant type contact areas in alternation and extend linearly between adjacent trenches.

10. The method of manufacturing a tenched field effect transistor of claim 7 wherein the implanting step for forming the source regions comprises implanting a first dopant at a first energy and dosage and a second dopant at a second energy and dosage, the second energy and dosage being less than the first energy and dosage, respectively.

11. The method of manufacturing a trenched field effect transistor of claim 7 wherein the heavy bodies are formed prior to forming the source regions.

12. The method of manufacturing a trenched field effect transistor of claim 7 wherein the source regions are formed prior to the heavy bodies.

13. The method of manufacturing a trenched field effect transistor of claim 7 further comprising a step of forming a field termination structure around a periphery of the field effect transistor.

14. The method of manufacturing a trenched field effect transistor of claim 13 wherein said field termination structure is formed by forming a deep well doped with a dopant of the second dopant type.

15. The method of manufacturing a trenched field effect transistor of claim 7 wherein said dielectric is applied before the steps of forming the heavy bodies and second dopant type contact areas, and the dielectric provides a mask for the patterning of the heavy bodies and second dopant type contacts.

16. The method of claim 1 wherein said third dopant comprises boron and said third dosage is from about 1E14 to 1E15cm^{-2}.

17. The method of claim 16 wherein said third energy is from about 20 to 40 keV.

18. The method of manufacturing a trenched field effect transistor of claim 13 wherein said field terminations structure is formed by forming a trench ring.

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(12) **United States Patent**
Mo et al.

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(54) **FIELD EFFECT TRANSISTOR AND METHOD OF ITS MANUFACTURE**

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(73) Assignee: **Fairchild Semiconductor Corporation**, South Portland, ME (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 35 days.

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(63) Continuation of application No. 08/970,221, filed on Nov. 14, 1997, now Pat. No. 6,429,481.

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(52) **U.S. Cl.** **257/341**; 257/331
(58) **Field of Search** 257/331, 341

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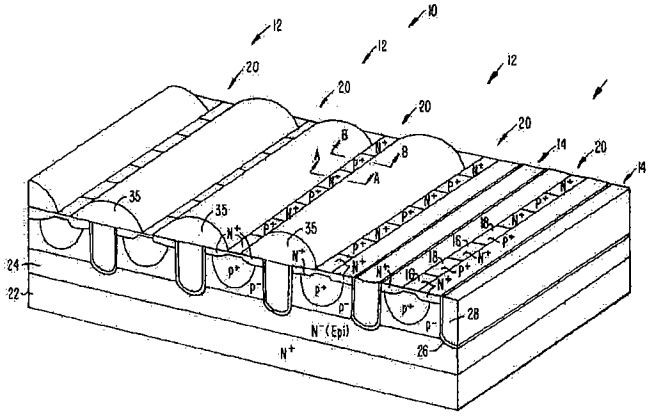
(57) **ABSTRACT**

A trenched field effect transistor is provided that includes (a) a semiconductor substrate, (b) a trench extending a predetermined depth into the semiconductor substrate, (c) a pair of doped source junctions, positioned on opposite sides of the trench, (d) a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of the heavy body extending less deeply into said semiconductor substrate than the predetermined depth of the trench, and (e) a doped well surrounding the heavy body beneath the heavy body.

32 Claims, 9 Drawing Sheets



30 to 100 keV and a dosage of 1E13 to 1E15, and driving it in to a depth of from about 1 to 3 μm using conventional drive in techniques.

The next two steps (p+ heavy body formation) can be performed either before formation of the n+ source junction, or afterwards, as indicated by the arrows in FIG. **3**. P+ heavy body formation and n+ source junction formation can be performed in either order because they are both resist-masked steps and because there is no diffusion step in between. This advantageously allows significant process flexibility. The p+ heavy body formation steps will be described below as being performed prior to source formation; it will be understood that n+ source formation could be performed first simply by changing the order of the steps discussed below.

First, a mask is formed over the areas that will not be doped to p+, as shown in FIG. **4***h*. (It is noted that this masking step is not required if the p+ heavy body is formed later, after the dielectric layer has been applied and patterned for contact holes. (see FIG. **4***k*, below) so that the dielectric itself provides a mask.) As discussed above, it is preferred that the junction at the interface between the p− well and the p+ heavy body be abrupt. To accomplish this, a double implant of dopant (e.g., boron) is performed. For example, a preferred double implant is a first boron implant at an energy of 150 to 200 keV and a dose of 1E15 to 5E15 cm^{-2}, and a second boron implant at an energy of 20 to 40 keV and a dose of 1E14 to 1E15 cm^{-2}. The high energy first implant brings the p+ heavy body as deep as possible into the substrate, so that it will not compensate the n+ source junction to be introduced later. The second, lower energy/lower dose implant extends the p+ heavy body from the deep region formed during the first implant up to the substrate surface to provide the p+ contact **18**. The resulting p+ heavy body junction is preferably about 0.4 to 1 μm deep at this stage of the process (final junction depth after drive-in is preferably about 0.5 to 1.5 μm deep), and includes a region of high dopant concentration near the interface with the p-well, and a region of relatively low dopant concentration at the contact surface of the p+ heavy body. A preferred concentration distribution is shown in FIG. **5**.

It will be appreciated by those skilled in the art that the abrupt junction can be formed in many other ways, e.g., by diffused dopants, by using a continuous dopant source at the surface or by using atoms that diffuse slowly.

After the formation of the p+ heavy body, a conventional resist strip process is performed to remove the mask, and a new mask is patterned to prepare the substrate for the formation of the n+ source junction. This mask is a n+ blocking mask and is patterned to cover the areas of the substrate surface which are to provide p+ contacts **18** (FIGS. **1** and **1***b*), as shown in FIG. **4***i*. This results in the formation of alternating p+ and n+ contacts after n-type doping (see lines A—A and B—B and cross-sectional views A—A and B—B in FIG. 4I, which correspond to FIGS. **1***a* and **1***b*).

The n+ source regions and n+ contact are then formed using a double implant. For example, a preferred double implant process is a first implant of arsenic at an energy of 80 to 120 keV and a dose of 5E15 to 1E16 cm^{-2} followed by a second implant of phosphorus at an energy of 40 to 70 keV and a dose of 1E15 to 5E15 cm^{-2} The phosphorus implant forms a relatively deep n+ source junction, which allows more process flexibility in the depth of the polysilicon recess, as discussed above. Phosphorus ions will penetrate deeper into the substrate during implant and also during later diffusion steps. Advantageously, the n+ source regions will have a depth of about 0.4 to 0.8 μm after diffusion. The arsenic implant extends the n+ source to the substrate surface, and also forms the n+ contacts **16** (see FIGS. **1** and **1***a*) by compensating (converting) the p-type surface of the p+ heavy body to n-type in the desired contact area. The preferred sheet resistance profiles for the n+ source along the edge of the trench, and the n+ contact are shown in FIGS. **5***a* and **5***b*, respectively.

Thus, the alternating p+ and n+ contacts **18**, **16**, shown in FIG. **1** are formed by patterning the substrate with appropriate masks and doping with the first p+ implant and the second n+ implant, respectively, as described above. This manner of forming the alternating contacts advantageously allows an open cell array having a smaller cell pitch than is typical for such arrays and thus a higher cell density and lower Rds_{on}.

Next, a conventional n+ drive is performed to activate the dopants. A short cycle is used, preferably 10 min at 900° C., so that activation occurs without excessive diffusion.

A dielectric material, e.g., borophosphate silicate glass (BPSG), is then deposited over the entire substrate surface and flowed in a conventional manner (FIG. **4***j*), after which the dielectric is patterned and etched (FIG. **4***k*) to define electrical contact openings over the n+ and p+ contacts **16**, **18**.

As noted above, the p+ heavy body implant steps can be performed at this point, if desired (rather than prior to n+ source formation), eliminating the need for a mask and thus reducing cost and process time.

Next, the dielectric is reflowed in an inert gas, e.g., a nitrogen purge. If the p+ body has been implanted immediately prior, this step is required to activate the p+ dopant. If the p+ body was implanted earlier, prior to the n+ drive, this step can be omitted if the dielectric surface is sufficiently smooth-edged around the contact openings.

The cell array is then completed by conventional metalization, passivation deposition and alloy steps, as is well know in the semiconductor field.

Other embodiments are within the claims. For example, while the description above is of an n-channel transistor, the processes of the invention could also be used to form a p-channel transistor. To accomplish this, "p" and "n" would simply be reversed in the above description, i.e., where "p" doping is specified above the region would be "n" doped instead, and vice versa.

What is claimed is:

1. A trenched field effect transistor comprising:

a semiconductor substrate having dopants of a first conductivity type;

a trench extending to a first depth into said semiconductor substrate;

a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;

a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a second depth that is less than said first depth of the trench; and

a heavy body formed in said doped well extending to a third depth that is less than said second depth of said doped well, the heavy body forming an abrupt junction with the well;

wherein, a location of the abrupt junction relative to the depth of the well is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.

2. The trenched field effect transistor of claim 1 wherein said doped well has a substantially flat bottom.

3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.

4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.

5. The trenched field effect transistor of claim 1 wherein the heavy body comprises a heavily doped region having dopants of the second conductivity type at the abrupt junction.

6. The trenched field effect transistor of claim 5 wherein the heavily doped region is formed by implanting dopants of the second conductivity type at approximately the third depth.

7. The trenched field effect transistor of claim 1 further comprising a deep doped region having dopants of the second conductivity type, the deep doped region extending into the substrate to a fourth depth that is deeper than said first depth of the trench.

8. The trenched field effect transistor of claim 7 wherein said deep doped region forms a PN junction diode with the substrate.

9. The trenched field effect transistor of claim 7 wherein the deep doped region forms a termination structure.

10. The trenched field effect transistor of claim 1 wherein the trench is lined with a dielectric layer and substantially filled with conductive material.

11. The trenched field effect transistor of claim 10 wherein the conductive material comprises polysilicon.

12. The trenched field effect transistor of claim 10 wherein the conductive material filling the trench is recessed relative to the surface of the semiconductor substrate.

13. A field effect transistor comprising:

a semiconductor substrate having dopants of a first conductivity type;

a plurality of gate-forming trenches arranged substantially parallel to each other, each trench extending to a first depth into said substrate, the space between adjacent trenches defining a contact area;

a pair of doped source junctions positioned on opposite sides of each trench, the source junctions having dopants of the first conductivity type;

a doped well having dopants of a second conductivity type with a charge opposite that of the first conductivity type, the doped well being formed in the semiconductor substrate between each pair of gate-forming trenches;

a heavy body formed inside the doped well and having a second depth that is less than the first depth of the trenches; and

heavy body contact regions defined at the surface of the semiconductor substrate along the length of the contact area,

wherein the heavy body forms an abrupt junction with the well, and the depth of the heavy body relative to a depth of the well is adjusted so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor.

14. The field effect transistor of claim 13, wherein each said doped well has a substantially flat bottom.

15. The field effect transistor of claim 13 wherein the adjusted depth of the junction causes the breakdown origination point to occur approximately halfway between adjacent gate-forming trenches.

16. The field effect transistor of claim 13 wherein each said doped well has a depth less than the first depth of said gate-forming trenches.

17. The field effect transistor of claim 13 wherein each said gate-forming trench has rounded top and bottom corners.

18. The field effect transistor of claim 13 further comprising a deep doped region having dopants of the second conductivity type, the deep doped region extending into the substrate to a depth greater than said first depth of the said plurality of gate-forming trenches.

19. The field effect transistor of claim 18 wherein the deep doped region forms a PN junction diode with the substrate.

20. The field effect transistor of claim 19 wherein the deep doped region forms a field termination structure surrounding the periphery of the plurality of gate-forming trenches.

21. The field effect transistor of claim 20 further comprising:

a layer of dielectric material formed over the deep doped region; and

a layer of conductive material formed on top of the layer of dielectric material.

22. The field effect transistor of claim 13 further comprising a field termination structure including a termination trench extending continuously around the periphery of the plurality of gate-forming trenches.

23. The field effect transistor of claim 22 wherein said field termination structure comprises a plurality of concentrically arranged termination trenches.

24. The field effect transistor of claim 13 wherein the heavy body forms a continuous doped region along substantially the entire length of said contact area.

25. The field effect transistor of claim 13 wherein said doped source regions extend along the length of the trench.

26. The field effect transistor of claim 25 further comprising a source contact region defined at the surface of the semiconductor substrate and configured to contacting the doped source regions.

27. The field effect transistor of claim 25 further comprising a plurality of source contact regions disposed along the length of the contact area in an alternating fashion with the plurality of heavy body contact regions.

28. The field effect transistor of claim 13 wherein between a pair of adjacent trenches, the heavy body is bounded by the pair of adjacent trenches and the doped source regions.

29. The field effect transistor of claim 13 wherein between a pair of adjacent trenches, the heavy body extends continuously parallel to the longitudinal axis of the trenches.

30. The field effect transistor of claim 13 further comprising:

a layer of dielectric lining inside walls of each of said plurality of gate-forming trenches; and

a layer of conductive material substantially filling the gate-forming trenches.

31. The field effect transistor of claim 30 wherein the layer of conductive material comprises polysilicon.

32. The field effect transistor of claim 30 wherein the top surface of the layer of conductive material substantially filling the gate-forming trenches is recessed relative to the top surface of the semiconductor substrate.

* * * * *

US006828195B2

(12) **United States Patent**
Mo et al.

(10) **Patent No.: US 6,828,195 B2**
(45) **Date of Patent: Dec. 7, 2004**

(54) **METHOD OF MANUFACTURING A TRENCH TRANSISTOR HAVING A HEAVY BODY REGION**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(22) Filed: **Jan. 17, 2003**

(65) **Prior Publication Data**

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Related U.S. Application Data

(60) Continuation of application No. 09/854,102, filed on May 9, 2001, now Pat. No. 6,521,497, which is a division of application No. 08/970,221, filed on Nov. 14, 1997, now Pat. No. 6,429,481.

(51) **Int. Cl.**[7] **H01L 21/336**

(52) **U.S. Cl.** **438/270**; 438/589

(58) **Field of Search** 438/270–272, 438/589

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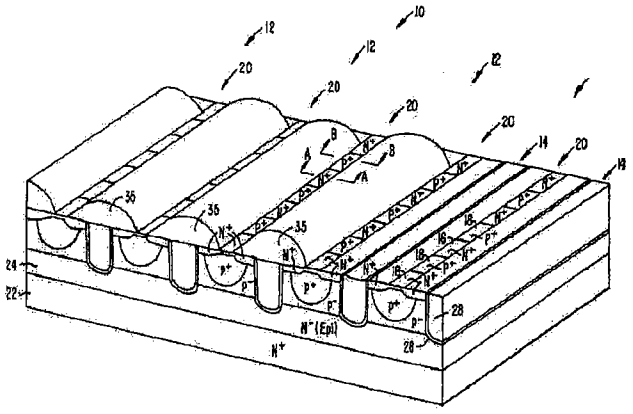
(57) **ABSTRACT**

A trenched field effect transistor is provided that includes (a) a semiconductor substrate, (b) a trench extending a predetermined depth into the semiconductor substrate, (c) a pair of doped source junctions, positioned on opposite sides of the trench, (d) a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of the heavy body extending less deeply into said semiconductor substrate than the predetermined depth of the trench, and (e) a doped well surrounding the heavy body beneath the heavy body.

23 Claims, 9 Drawing Sheets



flexibility. The p+ heavy body formation steps will be described below as being performed prior to source formation; it will be understood that n+ source formation could be performed first simply by changing the order of the steps discussed below.

First, a mask is formed over the areas that will not be doped to p+, as shown in FIG. **4***h*. (It is noted that this masking step is not required if the p+ heavy body is formed later, after the dielectric layer has been applied and patterned for contact holes. (see FIG. **4***k*, below) so that the dielectric itself provides a mask.) As discussed above, it is preferred that the junction at the interface between the p− well and the p+ heavy body be abrupt. To accomplish this, a double implant of dopant (e.g., boron) is performed. For example, a preferred double implant is a first boron implant at an energy of 150 to 200 keV and a dose of 1E15 to 5E15 cm^{-2}, and a second boron implant at an energy of 20 to 40 keV and a dose of 1E14 to 1E15 cm^{-2}. The high energy first implant brings the p+ heavy body as deep as possible into the substrate, so that it will not compensate the n+ source junction to be introduced later. The second, lower energy/lower dose implant extends the p+ heavy body from the deep region formed during the first implant up to the substrate surface to provide the p+ contact **18**. The resulting p+ heavy body junction is preferably about 0.4 to 1 μm deep at this stage of the process (final junction depth after drive-in is preferably about 0.5 to 1.5 μm deep), and includes a region of high dopant concentration near the interface with the p− well, and a region of relatively low dopant concentration at the contact surface of the p+ heavy body. A preferred concentration distribution is shown in FIG. **5**.

It will be appreciated by those skilled in the art that the abrupt junction can be formed in many other ways, e.g., by diffused dopants, by using a continuous dopant source at the surface or by using atoms that diffuse slowly.

After the formation of the p+ heavy body, a conventional resist strip process is performed to remove the mask, and a new mask is patterned to prepare the substrate for the formation of the n+ source junction. This mask is a n+ blocking mask and is patterned to cover the areas of the substrate surface which are to provide p+ contacts **18** (FIGS. **1** and **1***b*), as shown in FIG. **4***i*. This results in the formation of alternating p+ and n+ contacts after n-type doping (see lines A—A and B—B and cross-sectional views A—A and B—B in FIG. **4**I, which correspond to FIGS. **1***a* and **1***b*).

The n+ source regions and n+ contact are then formed using a double implant. For example, a preferred double implant process is a first implant of arsenic at an energy of 80 to 120 keV and a dose of 5E15 to 1E16 cm^{-2} followed by a second implant of phosphorus at an energy of 40 to 70 keV and a dose of 1E15 to 5E15 cm^{-2}. The phosphorus implant forms a relatively deep n+ source junction, which allows more process flexibility in the depth of the polysilicon recess, as discussed above. Phosphorus ions will penetrate deeper into the substrate during implant and also during later diffusion steps. Advantageously, the n+ source regions will have a depth of about 0.4 to 0.8 μm after diffusion. The arsenic implant extends the n+ source to the substrate surface, and also forms the n+ contacts **16** (see FIGS. **1** and **1***a*) by compensating (converting) the p-type surface of the p+ heavy body to n-type in the desired contact area. The preferred sheet resistance profiles for the n+ source along the edge of the trench, and the n+ contact are shown in FIGS. **5***a* and **5***b*, respectively.

Thus, the alternating p+ and n+ contacts **18**, **16**, shown in FIG. **1** are formed by patterning the substrate with appropriate masks and doping with the first p+ implant and the second n+ implant, respectively, as described above. This manner of forming the alternating contacts advantageously allows an open cell array having a smaller cell pitch than is typical for such arrays and thus a higher cell density and lower Rds_{on}.

Next, a conventional n+ drive is performed to activate the dopants. A short cycle is used, preferably 10 min at 900° C., so that activation occurs without excessive diffusion.

A dielectric material, e.g., borophosphate silicate glass (BPSG), is then deposited over the entire substrate surface and flowed in a conventional manner (FIG. **4***j*), after which the dielectric is patterned and etched (FIG. **4***k*) to define electrical contact openings over the n+ and p+ contacts **16**, **18**.

As noted above, the p+ heavy body implant steps can be performed at this point, if desired (rather than prior to n+ source formation), eliminating the need for a mask and thus reducing cost and process time.

Next, the dielectric is reflowed in an inert gas, e.g., a nitrogen purge. If the p+ body has been implanted immediately prior, this step is required to activate the p+ dopant. If the p+ body was implanted earlier, prior to the n+ drive, this step can be omitted if the dielectric surface is sufficiently smooth-edged around the contact openings.

The cell array is then completed by conventional metalization, passivation deposition and alloy steps, as is well know in the semiconductor field.

Other embodiments are within the claims. For example, while the description above is of an n-channel transistor, the processes of the invention could also be used to form a p-channel transistor. To accomplish this, "p" and "n" would simply be reversed in the above description, i.e., where "p" doping is specified above the region would be "n" doped instead, and vice versa.

What is claimed is:

1. A method of manufacturing a trench transistor comprising:

providing a semiconductor substrate having dopants of a first conductivity type;

forming a plurality of trenches extending to a first depth into the semiconductor substrate;

lining each of the plurality of trenches with a gate dielectric material;

substantially filling each dielectric-lined trench with conductive material;

forming a doped well in the substrate to a second depth that is less than said first depth of the plurality of trenches, the doped well having dopants of a second conductivity type opposite to said first conductivity type;

forming a heavy body extending inside the doped well to a third depth that is less than said second depth of said doped well, the heavy body having dopants of the second conductivity type and forming an abrupt junction with the well; and

forming a source region inside the well, the source region having dopants of the first conductivity types.

2. The method of claim **1** wherein the step of forming a doped well forms the well with a substantially flat bottom.

3. The method of claim **1** further comprising forming a deep doped region having dopants of the second conductivity type, the deep doped region extending into the substrate to a fourth depth that is deeper than said first depth of the trench.

4. The method of claim 3 wherein the step of forming a deep doped region forms a PN junction diode with the substrate that helps improve a breakdown voltage of the transistor.

5. The method of claim 3 wherein the deep doped region forms a termination structure around the periphery of the substrate.

6. The method of claim 1 wherein the step of substantially filling each dielectric-lined trench leaves a recess at an upper portion of each trench.

7. The method of claim 6 further comprising filling the recess at the upper portion of each trench with dielectric material.

8. The method of claim 1 wherein the step of forming the heavy body comprises a double implant process.

9. The method of claim 8 wherein the double implant process comprises:

a first implant of dopants of the first conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body; and

a second implant of dopants of the first conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body.

10. The method of claim 9 wherein the first implant occurs at approximately the third depth.

11. The method of claim 9 wherein the first energy level is higher than the second energy level.

12. The method of claim 11 wherein the first dosage is higher than the second dosage.

13. The method of claim 1 wherein the step of forming the heavy body comprises a process of diffusing dopants of the second conductivity type.

14. The method of claim 1 wherein the step of forming the heavy body comprises using a continuous dopant source at the surface of the semiconductor substrate.

15. The method of claim 1 wherein the step of forming a plurality of trenches comprises patterning and etching the plurality of trenches that extend in parallel along a longitudinal axis.

16. The method of claim 15 further comprising forming a contact area on the surface of the substrate between adjacent trenches.

17. The method of claim 16 wherein the step of forming the contact area comprises forming alternating source contact regions and heavy body contact regions.

18. The method of claim 16 wherein the step of forming the contact area comprises forming a ladder-shaped source contact region surrounding heavy body contact regions.

19. The method claim 18 wherein the step of forming the ladder-shaped source contact region surrounding heavy body contact regions, comprises:

forming a source blocking mask on the surface of the semiconductor substrate patterned to cover the heavy body contact regions; and

implanting dopants of the first conductivity type to form the ladder-shaped source contact region.

20. The method of claim 18 wherein the step of forming the ladder-shaped source contact region surrounding heavy body contact regions, comprises forming a dielectric layer on the surface of the semiconductor substrate patterned to expose the heavy body contact regions.

21. A method of manufacturing a trench field effect transistor on a semiconductor substrate having dopants of a first conductivity type, the method comprising:

etching a plurality of trenches into the semiconductor substrate to a first depth;

lining the plurality of trenches with dielectric layer;

substantially filling the dielectric-lined plurality of trenches with conductive material;

forming a well between adjacent trenches to a second depth that is shallower than the first depth, the well having dopants of second conductivity type opposite to the first conductivity type;

forming a heavy body inside the well to a third depth that is shallower than the second depth, the heavy body having dopants of the second conductivity type; and

forming a source region inside the well and adjacent to trenches, the source region having dopants of the first conductivity type,

wherein, the step of forming a heavy body employs a process to form an abrupt junction between the heavy body and the well at approximately the third depth.

22. The method of claim 21 further comprising adjusting a location of the abrupt junction relative to the depth of the well so that a transistor breakdown current is spaced away from the trench in the semiconductor.

23. The method of claim 21 further comprising forming a deep doped region having dopants of the second conductivity type, the deep doped region extending into the substrate to a fourth depth that is deeper than said first depth of the trench.

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US007148111B2

(12) **United States Patent**
Mo et al.

(10) **Patent No.: US 7,148,111 B2**
(45) **Date of Patent: *Dec. 12, 2006**

(54) **METHOD OF MANUFACTURING A TRENCH TRANSISTOR HAVING A HEAVY BODY REGION**

(75) Inventors: **Brian Sze-Ki Mo**, Fremont, CA (US); **Duc Chau**, San Jose, CA (US); **Steven Sapp**, Felton, CA (US); **Izak Bencuya**, Saratoga, CA (US); **Dean E. Probst**, West Jordan, UT (US)

(73) Assignee: **Fairchild Semiconductor Corporation**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **10/927,788**

(22) Filed: **Aug. 27, 2004**

(65) **Prior Publication Data**

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Related U.S. Application Data

(60) Continuation of application No. 10/347,254, filed on Jan. 17, 2003, now Pat. No. 6,828,195, which is a continuation of application No. 09/854,102, filed on May 9, 2001, now Pat. No. 6,521,497, which is a division of application No. 08/970,221, filed on Nov. 14, 1997, now Pat. No. 6,429,481.

(51) **Int. Cl.**
H01L 21/336 (2006.01)

(52) **U.S. Cl.** **438/270**; 438/272; 438/589

(58) **Field of Classification Search** 438/270, 438/272, 589

See application file for complete search history.

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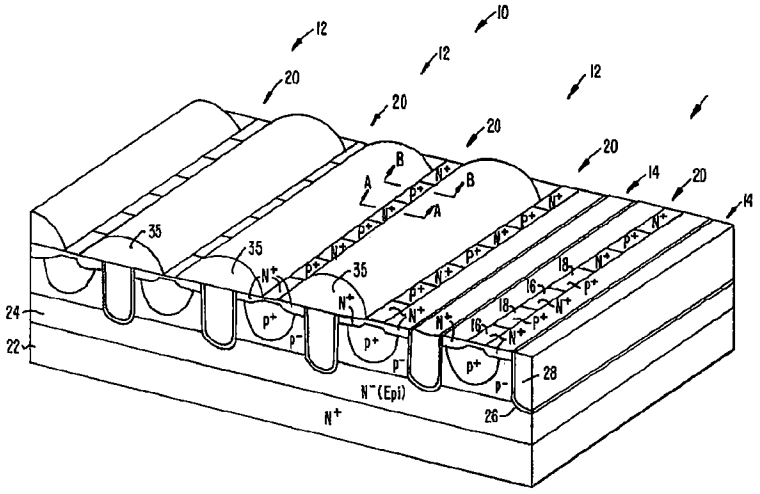
(57) **ABSTRACT**

A trenched field effect transistor is provided that includes (a) a semiconductor substrate, (b) a trench extending a predetermined depth into the semiconductor substrate, (c) a pair of doped source junctions, positioned on opposite sides of the trench, (d) a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of the heavy body extending less deeply into said semiconductor substrate than the predetermined depth of the trench, and (e) a doped well surrounding the heavy body beneath the heavy body.

36 Claims, 9 Drawing Sheets



performed in either order because they are both resist-masked steps and because there is no diffusion step in between. This advantageously allows significant process flexibility. The p+ heavy body formation steps will be described below as being performed prior to source formation; it will be understood that n+ source formation could be performed first simply by changing the order of the steps discussed below.

First, a mask is formed over the areas that will not be doped to p+, as shown in FIG. **4**H. (It is noted that this masking step is not required if the p+ heavy body is formed later, after the dielectric layer has been applied and patterned for contact holes. (see FIG. **4**K, below) so that the dielectric itself provides a mask.) As discussed above, it is preferred that the junction at the interface between the p– well and the p+ heavy body be abrupt. To accomplish this, a double implant of dopant (e.g., boron) is performed. For example, a preferred double implant is a first boron implant at an energy of 150 to 200 keV and a dose of 1E15 to 5E15 cm^{-2}, and a second boron implant at an energy of 20 to 40 keV and a dose of 1E14 to 1E15 cm^{-2}. The high energy first implant brings the p+ heavy body as deep as possible into the substrate, so that it will not compensate the n+ source junction to be introduced later. The second, lower energy/lower dose implant extends the p+ heavy body from the deep region formed during the first implant up to the substrate surface to provide the p+ contact **18**. The resulting p+ heavy body junction is preferably about 0.4 to 1 m deep at this stage of the process (final junction depth after drive-in is preferably about 0.5 to 1.5 m deep), and includes a region of high dopant concentration near the interface with the p-well, and a region of relatively low dopant concentration at the contact surface of the p+ heavy body. A preferred concentration distribution is shown in FIG. **5**.

It will be appreciated by those skilled in the art that the abrupt junction can be formed in many other ways, e.g., by diffused dopants, by using a continuous dopant source at the surface or by using atoms that diffuse slowly.

After the formation of the p+ heavy body, a conventional resist strip process is performed to remove the mask, and a new mask is patterned to prepare the substrate for the formation of the n+ source junction. This mask is a n+ blocking mask and is patterned to cover the areas of the substrate surface which are to provide p+ contacts **18** (FIGS. **1** and **1**B), as shown in FIG. **4**I. This results in the formation of alternating p+ and n+ contacts after n-type doping (see lines A—A and B—B and cross-sectional views A—A and B B in FIG. **4**I, which correspond to FIGS. **1**A and **1**B).

The n+ source regions and n+ contact are then formed using a double implant. For example, a preferred double implant process -is a first implant of arsenic at an energy of 80 to 120 keV and a dose of 5E15 to 1E16 cm^{-2} followed by a second implant of phosphorus at an energy of 40 to 70 keV and a dose of 1E15 to 5E15 cm^{-2}. The phosphorus implant forms a relatively deep n+ source junction, which allows more process flexibility in the depth of the polysilicon recess, as discussed above. Phosphorus ions will penetrate deeper into the substrate during implant and also during later diffusion steps. Advantageously, the n+ source regions will have a depth of about 0.4 to 0.8 m after diffusion. The arsenic implant extends the n+ source to the substrate surface, and also forms the n contacts **16** (see FIGS. 1 and **1**A) by compensating (converting) the p-type surface of the p+ heavy body to n-type in the desired contact area. The preferred sheet resistance profiles for the n+ source along the edge of the trench, and the n+ contact are shown in FIGS. **5**A and **5**B respectively.

Thus, the alternating p+ and n+ contacts **18**, **16**, shown in FIG. **1** are formed by patterning the substrate with appropriate masks and doping with the first p+ implant and the second n+ implant, respectively, as described above. This manner of forming the alternating contacts advantageously allows an open cell array having a smaller cell pitch than is typical for such arrays and thus a higher cell density and lower Rds_{on}.

Next, a conventional n+ drive is performed to activate the dopants. A short cycle is used, preferably 10 min at 900° C., so that activation occurs without excessive diffusion.

A dielectric material, e.g., borophosphate silicate glass (BPSG), is then deposited over the entire substrate surface and flowed in a conventional manner (FIG. **4**J), after which the dielectric is patterned and etched (FIG. **4**K) to define electrical contact openings over the n+ and p+ contacts **16**, **18**.

As noted above, the p+ heavy body implant steps can be performed at this point, if desired (rather than prior to n+ source formation), eliminating the need for a mask and thus reducing cost and process time.

Next, the dielectric is reflowed in an inert gas, e.g., a nitrogen purge. If the p+ body has been implanted immediately prior, this step is required to activate the p+ dopant. If the p+ body was implanted earlier, prior to the n+ drive, this step can be omitted if the dielectric surface is sufficiently smooth-edged around the contact openings.

The cell array is then completed by conventional metalization, passivation deposition and alloy steps, as is well known in the semiconductor field.

Other embodiments are within the claims. For example, while the description above is of an n-channel transistor, the processes of the invention could also be used to form a p-channel transistor. To accomplish this, "p" and "n" would simply be reversed in the above description, i.e., where "p" doping is specified above the region would be "if' doped instead, and vice versa.

The invention claimed is:

1. A method of manufacturing a trench transistor comprising:

providing a semiconductor substrate having dopants of a first conductivity type;

forming a plurality of trenches extending from a first surface of the substrate to a first depth into the semiconductor substrate;

lining each of the plurality of trenches with a gate dielectric material;

substantially filling each dielectric-lined trench with conductive material;

forming a doped well in the substrate to a second depth that is less than said first depth of the plurality of trenches, the doped well having dopants of a second conductivity type opposite to said first conductivity type;

forming a source region inside the doped well and extending to a third depth that is less than the second depth, the source region having dopants of the first conductivity type; and

forming a heavy body inside the doped well, the heavy body having dopants of the second conductivity type with a peak concentration occurring at a fourth depth below the third depth of the source region and above the second depth of the doped well.

2. The method of claim **1** wherein the step of forming a doped well forms the well with a substantially flat bottom.

3. The method of claim **1** further comprising forming a deep doped region having dopants of the second conductivity type, the deep doped region extending into the substrate to a fourth depth that is deeper than said first depth of the trench.

4. The method of claim 3 wherein the step of forming a deep doped region forms a PN junction diode with the substrate that helps improve a breakdown voltage of the transistor.

5. The method of claim 3 wherein the deep doped region forms a termination structure around the periphery of the substrate.

6. The method of claim 1 wherein the step of substantially filling each dielectric-lined trench leaves a recess at an upper portion of each trench.

7. The method of claim 6 further comprising filling the recess at the upper portion of each trench with dielectric material.

8. The method of claim 1 wherein the step of forming the heavy body comprises a double implant process.

9. The method of claim 8 wherein the double implant process comprises:

a first implant of dopants of the first conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body; and

a second implant of dopants of the first conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body.

10. The method of claim 9 wherein the first implant occurs at approximately the fourth depth.

11. The method of claim 9 wherein the first energy level is higher than the second energy level.

12. The method of claim 11 wherein the first dosage is higher than the second dosage.

13. The method of claim 1 wherein the step of forming the heavy body comprises a process of diffusing dopants of the second conductivity type.

14. The method of claim 1 wherein the step of forming the heavy body comprises using a continuous dopant source at the surface of the semiconductor substrate.

15. The method of claim 1 wherein the step of forming a plurality of trenches comprises patterning and etching the plurality of trenches that extend in parallel along a longitudinal axis.

16. The method of claim 15 further comprising forming a contact area on the surface of the substrate between adjacent trenches.

17. The method of claim 16 wherein the step of forming the contact area comprises forming alternating source contact regions and heavy body contact regions.

18. The method of claim 16 wherein the step of forming the contact area comprises forming a ladder-shaped source contact region surrounding heavy body contact regions.

19. The method of claim 18 wherein the step of forming the ladder-shaped source contact region surrounding heavy body contact regions, comprises:

forming a source blocking mask on the surface of the semiconductor substrate patterned to cover the heavy body contact regions; and

implanting dopants of the first conductivity type to form the ladder-shaped source contact region.

20. The method of claim 18 wherein the step of forming the ladder-shaped source contact region surrounding heavy body contact regions, comprises forming a dielectric layer on the surface of the semiconductor substrate patterned to expose the heavy body contact regions.

21. The method of claim 1 wherein the source region is formed prior to the heavy body.

22. The method of claim 1 wherein the step of providing a semiconductor substrate comprises:

forming a drain contact region at a second surface opposite to the first surface of the substrate; and

forming a substantially uniformly doped epitaxial layer atop said drain contact region.

23. A method of manufacturing a trench transistor comprising:

providing a semiconductor substrate having dopants of a first conductivity type;

forming a plurality of trenches extending from a first surface of the substrate to a first depth into the semiconductor substrate;

lining each of the plurality of trenches with a gate dielectric material;

substantially filling each dielectric-lined trench with conductive material;

forming a doped well in the substrate to a second depth that is less than said first depth of the plurality of trenches, the doped well having dopants of a second conductivity type opposite to said first conductivity type;

forming a source region inside the doped well to a third depth, the source region having dopants of the first conductivity type; and

forming a heavy body inside the doped well to a fourth depth between the third depth of the source region and the second depth of the doped well, the heavy body having dopants of the second conductivity type with a dopant concentration that is higher near the interface with the doped well than near the first surface.

24. The method of claim 23 further comprising forming a deep doped region having dopants of the second conductivity type, the deep doped region extending into the substrate to a fifth depth that is deeper than said first depth of the trench.

25. The method of claim 24 wherein the step of forming a deep doped region forms a PN junction diode with the substrate that helps improve a breakdown voltage of the transistor.

26. The method of claim 24 wherein the deep doped region forms a termination structure around the periphery of the substrate.

27. The method of claim 23 wherein the source region is formed prior to the heavy body.

28. The method of claim 23 wherein the step of providing a semiconductor substrate comprises:

forming a drain contact region at a second surface opposite to the first surface of the substrate; and

forming a substantially uniformly doped epitaxial layer atop said drain contact region.

29. A method of manufacturing a trench transistor comprising:

providing a semiconductor substrate having dopants of a first conductivity type, the semiconductor substrate including a first highly doped drain layer and a second more lightly and substantially uniformly doped epitaxial layer atop and adjacent the first layer;

forming a plurality of trenches extending to a first depth into the epitaxial layer, the plurality of trenches creating a respective plurality of epitaxial mesas;

lining each of the plurality of trenches with a gate dielectric material;

substantially filling each dielectric-lined trench with conductive material;

forming a plurality of doped wells in the plurality of epitaxial mesas, respectively to a second depth that is less than said first depth of the plurality of trenches, the plurality of doped wells having dopants of a second conductivity type opposite to said first conductivity type;

forming a plurality of source regions adjacent the plurality of trenches and inside the plurality of doped wells, the source regions having a third depth and dopants of the first conductivity type;

forming a plurality of heavy body regions each inside a respective one of the plurality of doped wells, each heavy body region having a fourth depth between the third depth of the source region and the second depth of the doped well, and having dopants of the second conductivity type; and

adjusting a dopant profile of the plurality of heavy body regions so that peak electric field is moved away from a nearby trench toward the heavy body resulting in avalanche current that is substantially uniformly distributed.

30. The method of claim **29** wherein the step of forming the plurality of heavy body regions comprises a double implant process.

31. The method of claim **30** wherein the double implant process comprises:

a first implant of dopants of the first conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body; and

a second implant of dopants of the first conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body.

32. The method of claim **31** wherein the first implant occurs at approximately the fourth depth.

33. The method of claim **31** wherein the first energy level is higher than the second energy level.

34. The method of claim **33** wherein the first dosage is higher than the second dosage.

35. The method of claim **29** wherein the step of forming the plurality of heavy body regions comprises a process of diffusing dopants of the second conductivity type.

36. The method of claim **29** wherein the step of forming the plurality of heavy body regions comprises using a continuous dopant source at the surface of the semiconductor substrate.

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